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REVIEW PAPER ON DECODING OF LDPC CODE USING ADVANCED GALLAGERS ALGORITHM

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Abstract— In this paper, we present energy-efficient architectures for decoder of low density parity check codes. This algorithm offer significant intrinsic advantages in the energy domain: computational complexity is lower, lower interconnect complexity, and very high throughput, also achieving error correction performance within limited SNR. We are presenting a fully parallel implementation for (2048, 1723) LDPC encoder and decoder code specified in the IEEE 802.3an (10GBASE-T) standard using Gallager's algorithm.

Keywords— LDPC Codes, BER, LLR Values.

I. INTRODUCTION

A low-density parity check [1] code is a linear error correcting code, a method of transmitting a message over a noisy transmission channel. Low-Density Parity Check (LDPC) codes were first proposed by Gallager in 1962. LDPC codes can achieve good Bit Error Rate (BER) than Shannon limit. LDPC code employed in 10Gbps Ethernet communication (IEEE standard 802.3an) [9].LDPC codes widely used in satellite TV transmission, space communication, magnetic storage in hard disk drive. Belief propagation algorithm is first decoding algorithm of LDPC code but it contains complex check node computation.

To simplify these computation in BP algorithm, min-sum algorithm (MSA) introduced by Fossorier [2]. Min-sum algorithm reduces the complexity by simplifying the check node computation but cannot improve the decoding performance of LDPC codes. To achieve the better decoding performance normalized min-sum (NMS) and Offset min-sum (OMS) algorithm introduced [3]. But decoding performance suffer from degradation when output near to zero, to solve this problem a modified offset min-sum algorithm (MOMSA) introduced [4]. The Min-Sum algorithm can provide similar performance to the ideal implementation with far lower computational complexity.

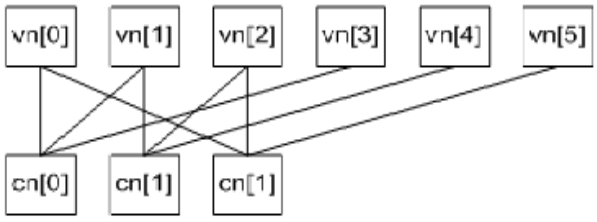
Rather than combining the likelihood values optimally in the check nodes for each edge, the Min-Sum algorithm uses the least likely received message as an approximation of the result for all edges but one. The message created for the edge which transferred the smallest LLR must be calculated separately, since the received result on any edge may not be used in the calculation of the message that will flow back along that same edge. For the edge that transferred the smallest LLR, the next-to-smallest LLR is used as an approximation. The Min-Sum approach allows for simpler arithmetic and reduces storage requirements, since only two LLR values are stored.

II. GENERALIZED LDPC DECODER AND MESSAGE PASSING

2.1 Tanner Graph

LDPC code has parity check matrix H with a small number of nonzero elements in each row and column. LDPC codes are defined by a sparse parity-check matrix H, which can be modeled by a Tanner graph where bit nodes (variable n) and check nodes (n-k) are connected by edges.

Fig 1 shows Simple Tanner Graph. A Tanner graph can be formed from the received bits ("variable nodes," or VN's) and the parity equations ("check nodes," or CN's). The parity equations, shown below the Tanner graph, are used to define the edges in the graph.



vn[3] = p[0] = vn[0] ^ vn[1]
vn[4] = p[1] = vn[1] ^ vn[2]
vn[5] = p[2] = vn[0] ^ vn[2]

Fig 1 : Simple Tanner Graph

In the BP algorithm, parity bits and likelihood values are passed as messages from all variable nodes to all connected check nodes. The initial likelihood values are derived from the channel quality and the Euclidian distance between the received symbols and the nearest constellation points. Messages are passed as log-likelihood ratios (LLR's), since representing probability ratios in this form allows for simpler arithmetic. The expected parity bits are passed to each connected variable node, along

with likelihood values. The VN's in turn use these values to update the VN parity bits and likelihood values, and the cycle begins again. In this way, the messages tend to strengthen bits which are in agreement with parity equations and correct bits which are in error.

2.2 Message Passing

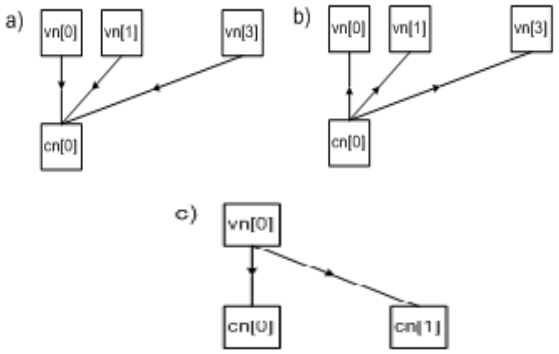


Fig 2 : Message passing

Fig 1 shows Message Passing. In (a), parity bits and likelihood ratios are passed from the variable nodes to the check nodes. In (b), the received messages are combined to create messages for the variable nodes, containing most likely parity values and the likelihood of that value being correct, based on the messages received from the other VN's. (c) shows how the variable nodes (in this case, VN[0]) uses the received data to send updated parity values and likelihood ratios.

III. VARIOUS DECODING ALGORITHM

Min-sum algorithm is two phase message passing LDPC decoding algorithm, first phase is variable node to check node message which shows that LLR values computed and sent to check nodes. Second phase is check node to variable node message are computed and send back to variable node [2].

To simplify the min-sum, improved algorithms proposed normalized min-sum (NMS) and offset min-sum. For NMS, normalize factor $1/\alpha$ can simplify check node computation equation but when output close to zero, decoding performance degraded. For OMS, offset factor or correction factor does not change according to output value and subtracted from minimum value but cannot achieve better improvement in performance [3].

Modified offset min-sum algorithm uses check node computation value to modify offset factor in each decoding step [4].Two more multiplication operation and P more addition are required in OMS algorithm where as MOMS require only P+2 more addition operation and it not increases hardware complexity [4].

Single minimum min-sum algorithm smMS modifies the check node update of MS algorithm. In some cases performance of smMS algorithm not good hence modifications are done in [6].This algorithm provides better BER performance than smMS algorithm. It gives error floor free operation below BER=10^{-15}.

If the signal to noise ratio (SNR) increases, error rate of LDPC decreases rapidly [7]. Growth rate of error pattern in absorbing set can be balanced by growth of the LLR's external to the set if a sufficient dynamic range is available to represent message/CFM (Bit node/Check node fractional module) perform computation at variable node and check node into sequentially [8][9][10]. Use of LLR values decreases number of computation and minimizes message storing memories.

IV. PROPOSED TECHNIQUE

In this paper, the Galleger's algorithm is used to present energy-efficient architectures for decoder of low density parity check codes. We are presenting a fully parallel implementation for (2048,1723) LDPC encoder and decoder code specified in the IEEE 802.3an (10GBASE-T) standard using Gallagher's algorithm. Single-port RAM's were used, requiring 2 cycles for each message transmission, but using less silicon and allowing more flexibility in terms of folding logic or multi-cycle paths, compared to dual-port RAM's. Using dual-port RAM's could allow for 180x, 90x or 45x parallelism for reduced area, with some increase in the complexity of the control logic [11][12].

The VN's are each connected to two RAM's, one holding the LLR values and one holding the sum of the incoming messages from the CN's. Each VN holds adders to combine incoming messages and create the outgoing message, and registers to hold the I/O data and the messages[13].

The CN's are each connected to a single, wide RAM holding the two smallest of the incoming LLR's during the current iteration, the signs of all incoming messages, the locations of the minimum values, and the parity result of all the incoming messages. The message to the VN's are produced by reading one of the two min-LLR values, along with the expected sign value for a particular edge.

The control module reads a ROM to fetch a shift value for the shuffle network and a write/read address for the check nodes. In the forward direction, for message passing from VN's to

CN's, these values are used directly. In the reverse direction, the shift value is negated to allow messages to flow along the same edge in both directions.

V. CONCLUSION

This paper presents the designing of LDPC decoder using Gallager's algorithm. The proposed decoder reduces Bit error rate and hence the hardware complexity. The proposed Gallager's algorithm reduces the computational complexity and gives higher throughput. The RAM's used at the CN's were wide enough to store information for the highest coding rates, and deep enough to store all messages for the lowest rates. This approach sacrificed area for maximal throughput, even though performance greatly exceeded requirements for most code rates. Also achieving error correction performance within limited SNR.

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